FERROELECTRIC La-Sr-Co-O / Pb-Zr-Ti-O / La-Sr-Co-O
HETEROSTRUCTURES ON SILICON

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Abstract: Ferroelectric Pb_{0.9}La_{0.1}Zr_{0.2}Ti_{0.8}O_{3} thin film capacitors with symmetrical La-Sr-Co-O top and bottom electrodes have been grown on [001] Si with a Yttria stabilized zirconia (YSZ) buffer layer and on SiO_{2}/Si substrates. A layered perovskite "template" layer (300 - 500Å thick), grown between the YSZ buffer layer or the SiO_{2} layer and the bottom La-Sr-Co-O electrode, is critical for obtaining the required orientation of the subsequent layers. The fatigue, retention and aging characteristics of these new structures are quite desirable for nonvolatile memory operation. Preliminary studies show that this ferroelectric performance obtained in large (50 - 100 μm diameter) capacitors can be replicated in smaller capacitors (down to 4 μm diameter) processed by ion milling.

INTRODUCTION

Ferroelectric thin film materials have had a strong resurgence in research and development recently, primarily because of their potential use as non-volatile, random access memories integrated with existing Si CMOS transistor circuitry\(^1\)\(^{-4}\). Conventionally the ferroelectric thin films, such as lead zirconate titanate (PZT), are deposited onto Pt coated Si wafers with Pt top contact electrodes to form the capacitor structure. Thin film deposition techniques including sol-gel spin-on, sputtering, chemical vapor deposition, and pulsed laser deposition are being used to deposit the thin films. Solutions to reliability issues such as fatigue, aging, retention and imprinting are being explored concurrently with issues related to integration with CMOS drive circuitry\(^5\)\(^{-10}\) and scaling down to dimensions that are commensurate with the requirements of high density nonvolatile memory technology.
Recent studies have shown that metal oxide electrodes yield capacitors with better fatigue properties compared to conventionally used Pt electrodes\textsuperscript{11-13}. Specifically, it has been demonstrated that the superconducting cuprates such as Y-Ba-Cu-O (YBCO), which are metallic at room temperatures, can be used as top and bottom electrodes. The capacitors so formed show very little bipolar fatigue\textsuperscript{13}. The YBCO top and bottom electrodes in these capacitors are typically grown in the temperature regime of 700-800 °C, which is higher than that conventionally used in Si process technology (about 550 °C). In an effort to reduce the growth temperature, we have been studying a variety of other metallic perovskite compounds as potential candidates for the top and bottom electrodes. Among such oxides, the cubic perovskite La-Sr-Co-O (LSCO) has been shown to have desirable metallic properties (room temperature resistivity as low as 90 μohm-cm) in recent studies wherein the thin film heterostructures were grown on single crystalline oxide substrates (SrTiO\textsubscript{3})\textsuperscript{12}. Even though LSCO is metallic and has good structural compatibility with the SrTiO\textsubscript{3} substrates used, in order to be useful in integrated ferroelectric memories, the capacitors have to be grown on Si wafers.

The capacitor structures are grown by pulsed excimer laser deposition onto [001] Si which is buffered with yttria stabilized zirconia (YSZ) surface layer or a thermally oxidized Si substrate. The important feature of this approach is that it can be carried out at a substrate heater temperature of 550 °C - 640 °C, (substrate temperature is approximately 50 °C lower) which is substantially lower than the previously reported range of 700 - 800 °C for YBCO top and bottom electrodes\textsuperscript{13}. The details of the deposition conditions are similar to that reported for the capacitors with YBCO top and bottom electrodes. Direct deposition of the LSCO/PLZT/LSCO layer onto the YSZ buffer layer yielded a [110] oriented film and capacitors fabricated from this heterostructure were only weakly ferroelectric. We attribute the strong [110] orientation to the large difference in lattice parameters between YSZ (5.16 Å) and LSCO (3.82 Å), which is detrimental for a simple cube-on-cube orientation relationship. This problem also exists in the case of direct deposition onto the thermally oxidized Si surface, in which case we observe a strong tendency for a chemical reaction (i.e., formation of the silicate) and consequently weak x-ray peaks for the perovskite LSCO phase.

This problem in both cases was overcome through the use of a very thin (approximately 300-500 Å) layer of c-axis oriented Bi\textsubscript{4}Ti\textsubscript{3}O\textsubscript{12}, which is not conducting and acts as a perovskite "template" layer. This template layer is also grown at the same growth temperature, i.e., 640 °C (in the case of the thermally oxidized Si substrate, the Bi\textsubscript{4}Ti\textsubscript{3}O\textsubscript{12} layer is grown at 670 °C). Due to its strong
structural anisotropy, Bi$_4$Ti$_3$O$_{12}$ grows in the c-axis orientation and provides a surface that is suitable for the growth of the subsequent LSCO and PLZT layers. The LSCO top and bottom electrodes were 1000 Å thick while the PLZT layer was 2700 Å thick. With such a "template" layer, the LSCO/PLZT/LSCO heterostructure is c-axis oriented. X-ray rocking curves about the 001 Bragg peak of the PLZT layer yielded a full width at half maximum of 0.7 - 0.8° in the case of the heterostructures grown on YSZ/Si and 1.1 - 1.5° in the case of the heterostructures grown on thermally oxidized Si. Rutherford backscattering analysis confirmed the composition of the various layers to be commensurate with that of the target, and no lead loss was observed as long as the substrate heater temperature was kept below 650 °C.

Test capacitors were fabricated using a shadow mask with areas in the range of 2x10$^{-5}$ - 10$^{-4}$ cm$^2$. Capacitors with areas smaller than 2x10$^{-5}$ cm$^2$ were fabricated using room temperature Argon ion milling. By this technique, we have been able to delineate 4 μm diameter capacitors so far. Electrical measurements were made using the Radiant Technologies tester, RT66A, in conjunction with a pulse generator. Pulsed polarization and hysteresis measurements were carried out using the sequence of pulses shown in the inset to Figure 1. For the bipolar fatigue experiments, internally generated 8.65 μsec wide square pulses or externally generated square pulses were used. After the end of each fatigue period, the polarization characteristics of the capacitors were measured using the same pulse sequence shown in the inset to Figure 1. Bipolar fatigue over a range of test frequencies and test temperatures, logic state retention and aging experiments were carried out on these capacitors to study their reliability characteristics. These experiments were performed on capacitors with the smallest area, to minimize the RC time constant.

FATIGUE

Figure 1 compares pulsed hysteresis loops from 50 μm x 50 μm capacitors grown on YSZ/Si and SiO$_2$/Si and on single crystal LaAlO$_3$. The [001] oriented films grown on the bismuth titanate "template" show clear ferroelectric hysteresis loops. The coercive fields are in the range of 25 - 50 kV/cm, corresponding to coercive voltages of 0.6 - 1.2 V. Pulse polarization measurements show that the capacitors have remnant polarizations (defined as ΔP=switched polarization - non-switched polarization, both being measured at the bottom of the pulse) in the range of 8 - 35 μC/cm$^2$ (depending upon the applied voltage and the substrate).

Figure 2 shows the results of the bipolar fatigue experiments at two frequencies, 20 kHz and 1 MHz, both at ±3 V. For example, at 1 MHz, there is approximately 10
% loss of remnant polarization after $10^{12}$ bipolar cycles. Fatigue testing at higher voltages, i.e., 5 V, yielded a similar behavior as a function of fatigue cycles. Pulse polarization studies after the fatigue experiment show that this 10% loss of polarization is reversible by poling for longer times at the cycling voltage. An important observation is that the trend is quite similar for the three types of capacitors, as shown in Figure 3, although the switched polarization values are smaller for the
FIGURE 2  Fatigue of LSCO/PLZT/LSCO capacitors grown on YSZ/Si with a template layer at two frequencies, 20 kHz and 1 MHz.

FIGURE 3  Fatigue of LSCO/PLZT/LSCO capacitors grown on single crystal LaAlO$_3$, YSZ/Si with the bismuth titanate "template" layer and thermally oxidized Si with the bismuth titanate "template" layer.
capacitors grown on SiO2/Si. This fatigue behavior is consistent with earlier results from test capacitors with Y-Ba-Cu-O top and bottom electrodes as well as those with RuO2 electrodes11-13.

The exact reasons for the superior fatigue characteristics of capacitors with metallic oxide top and bottom electrodes as compared to Pt electrodes is not clear. We attribute the better performance to the difference in the nature of the electrode-ferroelectric interface and not to phenomena occurring in the bulk. Evidence in the support of this interpretation is the fact that when the top LSCO is replaced by a Pt electrode, the capacitors fatigue dramatically. These results are also consistent with what was observed in the case of Y-Ba-Cu-O electrodes13.

Capacitance-voltage (C-V) measurements (which are mainly sensitive to domain walls and their displacement under low bias fields) on the test capacitors before and after the fatigue test show a qualitatively similar behavior, as shown in Figure 4, although the overall signal drops by about 10 % after fatiguing for 1011 cycles, corresponding to the approximately 10 % drop in remnant polarization after the fatigue test. This suggests that there is still a small degree of domain wall pinning in the capacitors during the fatigue test period, which leads to the loss of remnant polarization.

![Figure 4](image)

FIGURE 4 Capacitance vs. voltage characteristics of the LSCO/PLZT/LSCO capacitor grown on YSZ/Si with a template layer before and after fatigue.
RETENTION AND AGING

We then studied the logic state retention and aging characteristics of the test capacitors. The retention experiments were typically carried out using a write voltage of ±3 V, with a pulse width of 8.6 μs. The read pulse is 2 ms wide and is of variable amplitude (typically 2.5 V). The polarization values at the top (i.e., at the maximum read voltage) and at the bottom (i.e., when the read voltage is zero) of the read pulse are measured. Figure 5 shows the results of a typical retention test over five decades of time for a LSCO/PLZT/LSCO capacitor grown on YSZ/Si substrate. Polarization values for both the logic state "1" (write/read pulses of opposite polarity) and the logic "0" (write/read pulses of the same polarity) are plotted in this figure. Under these test conditions, we find that there is more than sufficient difference (approx. 10 - 15 μC/cm²) in polarization values between the two states. Pulsed hysteresis loops and polarization measured before and after the retention test for both the logic states show no difference in shape and magnitude. The trend is similar in the case of capacitors grown on SiO₂/Si substrates, although the difference between logic "1" and logic "0" is smaller (about 6 - 8 μC/cm²).

FIGURE 5 Logic state retention for the LSCO/PLZT/LSCO capacitor after fatiguing for 10¹² cycles. The write voltages are ±3 V and the read voltage is 2.5 V. The capacitor shows sufficient distinction (~13 μC/cm²) between these two states. Open marks correspond to polarization values in the saturation condition and filled marks correspond to polarization values in the remnant condition.
Another property related to the fatigue and retention characteristics of these capacitors is aging. Aging is the loss of switchable polarization with shelf life (i.e., there is no dynamic and repeated polarization reversal involved). In this test, the capacitor is poled into one of the remnant states (for example, -P_r) for a certain period of time after which it is read with a sequence of pulses identical to that used to measure the pulse polarization value (as shown in the inset to Figure 1). The read pulse sequence measures the switched and nonswitched polarization values in both the polarization directions. Figure 6 shows aging data for capacitors grown on YSZ/Si and SiO_2/Si, and on single crystal LaAlO_3. In this particular case, the write voltage

\[ V_{\text{write}} = -3 \, \text{V}; \quad V_{\text{read}} = \pm 2.5 \, \text{V} \]

was -3 V (write pulse width of 8.6 μsec) and the read pulses were ±2.5 V (2 msec pulse width). We typically observe a weak log-linear drop in the remnant polarization (i.e., switched - nonswitched polarization) with aging time, consistent with what is generally observed in bulk PZT ferroelectrics.

**FIGURE 6** Aging of the LSCO/PLZT/LSCO capacitors grown on YSZ/Si and SiO_2/Si with template layers, and single crystal LaAlO_3. The write voltage was -3 V with a pulse width of 8.6 μsec, and the read pulse were ±2.5 V with a pulse width of 2 msec.
HIGH TEMPERATURE TESTING

Concurrent with room temperature studies of the ferroelectric performance, we are also carrying out high temperature testing (upto 200 °C). These tests are being carried out for two important reasons: (i) firstly, in order to be used as the nonvolatile storage cell in a ferroelectric IC, the capacitors need to perform reliably over a range of temperatures, e.g., -55 °C - 85 °C; (ii) secondly, temperature dependent studies of fatigue and aging will yield characteristic activation energies for the transport of species such as oxygen vacancies which may, in turn, be responsible for the loss of polarization during bipolar cycling or during aging.

Figure 7 shows a plot of switched (P*) and nonswitched (P^) remnant polarizations as a function of temperature for a capacitor grown on YSZ/Si. The nonswitched polarization is in general independent of temperature over the range of interest, i.e., room temperature to 150 °C, while the switched polarization shows a monotonic drop with temperature. In Figure 8, the fatigue performance of a test capacitor at room temperature (32 °C) is compared with that at 100 °C, at a test frequency of 1MHz and ± 3V. The main difference between the data for the two
temperatures is that the remnant polarization at 100 °C is smaller than that at 32 °C, consistent with the drop shown in Figure 7. However, the overall fatigue behavior of the capacitors at 32 °C and 100 °C is almost identical, indicating that high temperature reliability, at least up to 100 °C is not an aspect of concern in these metal oxide capacitors.

AREA SCALING

While the ferroelectric performance of the test capacitors are quite desirable, as illustrated by the data in Figures 1-7, it is also important to examine the scaling of these ferroelectric properties with the area of the capacitors, since commercially viable memory applications will in all likelihood require high density (at least 1 Mbit chips) memory architectures, leading to capacitor size which are in the range of 2 - 5 µm in lateral dimensions. We are exploring this issue of scaling by fabricating capacitors in the size range of 2 - 32 µm diameter using Argon ion milling with and without chemical assistance. We are using SiO₂ as the interlevel dielectric to isolate the top and bottom electrodes.
FERROELECTRIC LSCO/PZT/LSCO HETEROSTRUCTURES ON Si

Preliminary results of these dry etching experiments have proved to be very encouraging. Pulsed hysteresis loops from these capacitors fabricated by ion milling show polarization values quite similar to those obtained from discrete 100 μm capacitors. The hysteresis loops from these smaller size capacitors have a linear component, as illustrated in Figure 9, due to the parasitic capacitance in the test circuitry which is comparable to that of the test capacitor. Fatigue data from a 4x4 array of 4 μm (nominal diameter) is shown in Figure 10. These capacitors also show similar fatigue behavior to 100 μm capacitors. However, the boundary conditions will be changed as the size of capacitors (lateral dimension) decreases to the order of capacitor thickness. This will in turn change internal electric field, which may affect polarization switching and further fatigue behavior of the capacitors. Further investigation on fatigue behavior of smaller capacitors is being carried out.

CONCLUSIONS

The growth of c-axis oriented ferroelectric PLZT capacitor structures on silicon with LSCO top and bottom electrodes has been demonstrated. For high quality c-axis oriented capacitors, a thin "template" layer consisting of a layered perovskite material
such as bismuth titanate, is required. All the layers are grown at a substrate heater temperature of 640 °C, which is considerably lower than that used to grow YBCO based capacitor heterostructures. The capacitors grown subsequent to the use of the template layer exhibit large switched polarization values enough for nonvolatile memory applications. Ion milled small capacitors (4 - 32 μm diameter) as well as discrete large (50 - 100 μm) test capacitors show fatigue, aging and logic state retention characteristics that are very desirable for reliable memory operation.

REFERENCES


FERROELECTRIC LSCO/PZT/LSCO HETEROSTRUCTURES ON Si