UTILIZING PROPAGATION DELAY TO MASK FUNDAMENTAL MODE OF
CRYSTAL CONTROLLED TTL GATE OSCILLATORS

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Abstract

A new method of masking the fundamental mode of MXO type oscillators utilizing propagation delay in Schottky TTL inverter will be discussed. This method does not require conventional traps made of inductors and capacitors. Also, will be discussed is a method of compensating for undesired phase shift due to propagation delay in Schottky TTL gate oscillators. Both of the above methods mentioned are achieved by selecting the proper number of gates in the oscillator loop.

Introduction

It is the purpose of this paper to discuss the results obtained from investigating the use of device propagation delay in crystal oscillator mode selection. The investigation utilized 74500 gates, however most of the information applies to other logic families as well. In the past propagation delay in logic devices being used as the gain element of a crystal oscillator has been seen as undesirable. It forced the designer to add components to the design to compensate for the effect of propagation delay. The propagation delay also limits the frequency at which logic gate type oscillators could operate at. In this paper we will discuss some methods by which propagation delay can be of benefit in trapping the third overtone response of a crystal.

Discussion of Method

The propagation delay of a Schottky TTL inverter is approximately 5 nano seconds. That propagation delay is equivalent to a phase shift at a specific frequency.

Phase = Prop X Freq X 360

The phase shift due to propagation delay increases proportionally with frequency as seen from equation one. At 50 MHz the 74500 which is a Schottky Nand gate, has approximately 90 degrees of phase shift due to its propagation delay and 180° of phase shift due to the inverting action. If the circuit was connected as in figure one, the crystal would have to supply +90° to run on f1 of the dual monolithic crystal or -90° to run on f2. Requiring the crystal to supply more than plus or minus 45° deviation from 0 (f1 mode) or 180 (f2 mode) degrees is undesirable due to increased insertion loss and lower rate of change of phase outside those ranges (See Figure Four).

A method of compensation has been found that not only maintains the phase around the loop within +/-45° of f1 or f2 mode but also can be used to trap out the fundamental mode so that third overtone oscillation can be achieved. In general there are multiple gates in logic I.C. so that no actual circuit parts are added if you use one gate or four gates. The circuit of figure two was developed with that in mind. With the circuit of figure two there are three ways a dual monolithic crystal can be connected to form an oscillator (See Figures Three through Five). If the phase of node two, three, and four with respect to one are plotted as a function of frequency graphs one through three show the results. The hashed areas are the frequency ranges in which the phase is within +/-45° of 180° or 360°. Inspection of the graphs reveals that one of the three circuits will yield a phase shift within +/-45° of 180 or 360 at any frequency.

Phase= #inv X Prop X Freq X 360 X #inv X 180

If the propagation delay is not 5 nS as used in these graphs the frequencies that each circuit will operate at will change accordingly but one of the circuits will still work. So that the problem of added phase lag around the oscillator loop due
to propagation delay can be solved by selecting the proper number of gates in the loop.

For the remainder of this discussion the frequency range will be limited to 26.5 - 73.5 MHz. By limiting the frequency from 26.5 - 73.5 MHz we decrease the maximum phase shift required of the crystal from +/-45° to +/-36° of 180 (f1) or 360 (f2). This will improve the ability of the circuits to trap out the fundamental mode. Graphs four and five are of the phase of nodes two and three with respect to node one vs. frequency respectively. The hashed areas are the frequency ranges in which the phase is within +/-36° of 180° or 360°. It can be seen from the graphs that when the third overtone frequency lies in the hashed area of a graph the fundamental frequency will not. Let's say for example, you need a 65 MHz 3rd overtone oscillator. That means that the fundamental mode of the crystal is at 21.667 MHz, now you go to graphs four and five and find the one that has the area of 65 MHz hashed in but not the area 21.667 MHz. You should find that figure five meets these guidelines. Since the fundamental mode is not in a hashed area, the oscillator should run on the third harmonic unless the third harmonic response of the crystal is greatly attenuated. If the crystal is physically constructed to be operated on its third overtone it can be expected to have a third overtone response at least equal to its fundamental. To insure that the oscillator runs on the third overtone the crystal should have a third overtone response that is at least 3 dB greater than the fundamental response.

Conclusion

The method of using propagation delay in a gate oscillator to trap out the fundamental, needs more investigation. Several oscillators have been constructed utilizing the above information and tested. The test units for the most part exhibited specifications typical of the MXO family. The greatest advantage of this method of trapping out the fundamental over other methods is the small physical size.
FIGURE 1

FIGURE 2

FIGURE 3
COUPLED DUAL MONOLITHIC RESONATOR

FIGURE 6

AMPLITUDE RESPONSE

PHASE RESPONSE