SUMMARY

Crystal devices for applications in space and underwater systems require very low failure rates. Planning for the development and manufacture of crystal devices for these low failure rate applications involves some special techniques. In this paper some of these special techniques are outlined and discussed.

These techniques are used to control both parametric (i.e., aging) and catastrophic (i.e., plate cracking or electrical connection failure) crystal device failures for the planned lifetime of the user system.

Emphasized in this paper is the fact that the device and manufacturing process must be designed together, using the best known available material interfaces and processing technologies. The use of new and untested crystal designs and manufacturing processes must be kept to an absolute minimum. Extra attention must be given to special and extensive qualification of any untested parts of the selected device fabrication technology.

Also emphasized in this paper is the difficult-to-achieve detailed and continuous cooperation between system customer and device manufacturer that is necessary to optimize the chance for a successful installed and operating system.

A very important part of the required qualification of the design of the device and of the associated manufacturing process is the design of the testing program on the appropriate number of devices fabricated with the designed process.

Useful mechanical and thermal tests are described. These tests and requirements include yields at several appropriate steps in the manufacturing process, failure modes and statistical characteristic failure values for various overstresses (i.e., mechanical vibration and shock, thermal, electrical, magnetic, etc.), and
temperature and electrical drive coefficients for various electrical properties of the crystal device such as resonance frequency or motional resistance.

An important tool for defining the reliability goals of a crystal device is a credible device cost versus failure risk curve. Some of the attributes of cost-risk curves are discussed.

A series of rules that need to be observed by all persons involved in the design, manufacture, and application of high reliability crystal devices are listed and used to discuss various parts of the planning process.

In the discussion of adequate process control, emphasis is placed on the definition and implementation of proper in-process checks and the maintenance of proper data files during the project lifetime. The process check data should confirm to the supplier and customer alike that any given shipped device was manufactured by the process previously qualified during the engineering development phase of the project.

Changes in any of the in-process or post-seal test results of any kind indicate that the process must be restored to that used in the qualification program. Permanent changes in test results require that a complete requalification of the changed process be performed.

Although the manufacture of high reliability crystal devices is very difficult, there is enough evidence to demonstrate that adherence to a proper set of rules enhances the prospects for a successful system application.

Five general references are listed in the last section of this paper. A more complete set of references is beyond the scope of this paper.

DEVICE RELIABILITY CONCEPTS

There are many ways to characterize the reliability of circuit components such as crystal devices. For the purposes of this paper the level of the device reliability is broadly defined by the kind of application for which it was designed.

Two extremes of device reliability are considered. At the ordinary levels of reliability are the lower cost devices used in consumer products and in some land-based systems. For these applications device repair or replacement can be accomplished at a cost that is modest compared to the device cost. In addition the cost of a system failure is relatively modest.
The highest level of reliability is that required for space systems and for underwater transmission systems.

For space systems the mission time is very variable at a few months to many years. Very severe environmental effects may be experienced at launch and then continuously or repeatedly (cosmic particles, shock, vibration, acceleration, etc.) during the mission. Device replacement is extremely difficult and therefore very costly. Very high system reliability can be achieved by using very reliable components in redundant system modules. The cost of a system failure is a costly mission failure.

For underwater systems device replacement is possible, but also very costly. System installation may involve severe environmental effects (mechanical shock and vibration and thermal gradients), but after the repeater is on the ocean floor, the system experiences almost no further effects of this type. Instead, chemical, humidity, and pressure effects are the main forces at work.

Usually the desired system operating lifetime is very long (> 20 years) and device parameter drifts (aging) become very important. Since the underwater systems are often high speed transmission systems with a large number of information channels, a system down time represents a considerable loss of revenue for the system owner.

Because a large fraction of the aging of most crystal devices occurs in the first few years, the lifetime needs of space and underwater systems can lead to very similar aging requirements on the crystal devices.

It must be recognized that many systems require devices with levels of reliability between the two extremes defined above. Some of the techniques discussed in this paper can be used to make a better cost-risk device for these systems.

**RELIABILITY REQUIREMENTS for SYSTEMS**

A common measure of device reliability is called a failure in time or a fit. One "fit" is defined as one failure in $10^9$ hours of device operation. Since one year is 8,760 hours, one fit may also be considered as one failure in about $1.14 \times 10^5$ years of single device operation. One fit may also be considered as one failure per year for $1.14 \times 10^5$ operating devices.
Although time and device count are often interchanged in the estimation of device failure rates, each device failure type must be examined separately to make certain that the time-count failure description is appropriate. There is usually no substitute for reliability studies on large numbers of devices.

The difficulty of making accurate failure rate estimates leads to a very important theorem in the business of selling and buying high reliability devices. This theorem says that extremely good communication between system customer and device supplier on risk and cost must continue through the entire system design, manufacture, installation, and service phases of the project. The difficulty of accurately assessing the risks means that the customer and device supplier must share the consequences of the final achieved or estimated level of risk. Both device supplier and system customer must work together diligently to come to terms with this issue of sharing the risk.

For example, at an early stage in the device supplier - system customer interaction, even before the budget and schedule for the project are finalized, it is important to define the desired reliability goals very carefully and accurately. An important tool in these discussions is a cost-reliability curve as shown in Figure 1. Figure 1 shows that devices with very high reliability will be very expensive, while devices with moderately high reliability do not cost very much more than devices with relatively low reliability. In Figure 1, each manufacturing technology has its own curve, so that costs also depend on choice of manufacturing technology as well. This dependence is illustrated by the two curves on the risk-cost chart shown in Figure 2. For example, if the manufacturing technology should need to be changed in the course of device manufacture, the device cost or reliability could change considerably, as process step yields and quality change. Device cost also depends on production volume and on production rate, and additional curves can be added to Figure 2 to illustrate the various cost-risk tradeoffs.

The need to monitor and control the manufacturing technology leads to extensive qualification programs at the beginning of the project and extensive technology monitoring programs throughout the manufacturing cycle.

It is important to be able to demonstrate with convincing evidence that the shipped product is similar in all important ways to the group of exhaustively tested product fabricated during the process qualification period.
The general ideas just discussed are now used to discuss some
details that have been found to be useful in planning for the
manufacture, sale, and application of high reliability devices.

**RULES and PLANS**

First, there must be rules about the process of designing,
manufacturing, and installing the devices into the operating system.

The first rule is therefore:

> There are rules.

The second rule is:

> There must be careful and continuing communication between device
supplier and system customer throughout the life cycle of the
project.

The third rule is:

> All people connected with the project must know, subscribe to,
and rigorously observe all of the rules. These people include
shipping people, device fabrication people, device and system
designers, customer assembly people, etc.

The fourth rule is:

> A written plan leading to the agreed upon desired reliability
goals must be formulated early in the project and subscribed to
by all supplier and customer people connected with the project.

This plan must include:

1. A project control schedule.

2. A detailed description of the basic technology to be used to
manufacture the devices. This includes a written detailed
process manufacturing layout.

3. A written list of all known and imagined device failure modes
with an estimated probability of occurrence for each mode. This
list will be associated with the particular device
manufacturing technology selected for the project. The list
will be updated during the project as more detailed failure
information becomes available. The purpose of this list is to
make certain that no reasonable failure modes are overlooked in
the project plan.
4. A set of quality control points at which the manufacturing process is quantitatively characterized or monitored to determine conformance to the process used to fabricate the devices studied in the qualification phase of the project.

5. A set of device tests that will quantitatively characterize the important device failure modes of devices made by the qualified manufacturing process. Included are tests to be imposed on all shipped product, such as device parameter changes due to thermal and mechanical shock and mechanical vibration, device parameter temperature coefficients, changes in device parameters due to mounting and sealing, and device parameter changes during preshipment electrical or thermal burn-in. Other stresses, such as electrical drive level changes, can be used to measure variable nonlinear behavior associated with uncontrolled fabrication process variations.

Destructive overstress tests can be used to characterize device failure modes during thermal and mechanical overshock, over amplitude vibration and wider vibration frequency ranges, thermal step stress, and isothermal aging. Other destructive device tests can be useful measures of device reliability. The particular forms of the device failures due to overstresses are a sensitive control check on the device design and manufacturing process.

6. A plan for the fabrication of a sufficient number of devices by the qualified process so that enough reliability tests can be performed to generate the proper level of confidence in both device supplier and system customer. For very low device failure rate goals (1 to 10 fits) it is vital that no unaccelerated failures occur during the process qualification or manufacturing phases of the project.

7. A plan for the generation and retention of proper records so that every shipped device has a documented pedigree with written records supporting the conformance of the manufacturing process to the earlier qualified fabrication process.

8. A plan for making changes to the plan.

As this kind of plan is implemented, the supplier gathers and stores and interprets (and the customer pays for) a large amount of information on fabrication process checks and device performance at many places in the fabrication process.
DESIGN and TESTS

The success of the project depends on both coordinated device and fabrication process designs based on experience and on careful attention to detail. Lack of attention to the design of either the device or of the process will surely compromise the necessary knowledge about the quality and reliability of the final shipped product.

After the manufacturing process has been qualified as having yielded devices that respond in known and acceptable ways to mechanical, electrical, and thermal stresses and overstresses, then even the internal process step yields and the final electrical and burn-in yields and parameter distributions become requirements in production. Any significant changes in yield or statistical parameter value distributions (better or worse) indicate changes in the process that require restoration to the original process or an expensive and lengthy process requalification. In addition, particular failure modes at appropriate levels of mechanical and thermal overshock, mechanical overvibration, and thermal or electrical step stress, also become requirements.

All material interfaces in the device must be designed and controlled. The crystal blank, electrodes, mounting, and package configuration must be designed to produce a minimum mechanical stress on the quartz plate. Any residual stresses present may lead to catastrophic or parameter drift device failure. All failures of this type must be accelerated during the reliability testing program to insure adequate control.

In this section some of the tests that have been used to characterize a manufacturing process for high reliability crystal devices are briefly discussed.

First, the package and crystal mounting and crystal plate must be designed and processed to maintain low levels of mechanical stress in the completed device. Any residual stress can result in long term parametric (aging) or catastrophic (plate or electrode cracks) device failures.

Second, water drop contact angle or steam condensation measurements on every batch of crystals cleaned for metallization are very useful in determining the constancy of the chemical and physical state of the crystal surface prior to metallization. These measurements can be correlated with surface physics measurements such as Auger spectroscopy, electron microscopy, X-ray emission, fluorescence, etc. to add physical understanding about the nature of the contaminants present.
Third, frequency drifts of crystal devices stored in the evacuated metallization system for several hours can be used to determine the cleanliness of the system. Other vacuum system tools include unpumped system leak back rate, pump down time during the metallization cycle, and surface cleanliness measurements on test specimens stored in the pumped or unpumped system for several hours. Pressure rise during the metallization process is also a significant measure of system performance and cleanliness.

Next, statistical analysis of values of destructive bond pulls on metallized parts or appropriate test samples can be used to monitor the metal film adhesion to the crystal surface as well as to characterize the bonding machine and process. In addition, these results assure continued mechanical integrity of device electrodes during system installation and use.

Statistical analyses of the resonance frequencies of mounted crystals as compared to a knowledge of the properties of the metallized crystal plate can give important information about the crystal mounting process. Large frequency shifts during mounting may signify excessive mounting stress or contamination. Both effects are likely to cause excessive crystal parameter aging. Mounting stress can also produce catastrophic crystal failures within the system lifetime.

In every case the package and crystal mounting process must be designed to minimize this stress, even if the device resonance frequency and other parameters are insensitive to the stress.

Changes in the frequency adjustment process can be monitored by statistical results on post-adjustment frequency drifts accelerated by thermal baking in vacuum.

Frequency shifts during the package sealing process can be used for some devices to indicate the control of crystal stress related to the sealing process. Again, if the device is insensitive to the stress, then this stress must be monitored and controlled in some other way, i.e., measurements on a stress sensitive part mounted and sealed by the same processes.

After the package is sealed, standard thermal and mechanical shock and mechanical vibration and thermal cycling can be used to assure device mechanical survival on subsequent shipment and installation for service.

Device parameter changes during a thermal and electrical burn-in can be used to establish the constancy of the produced product's performance on an important reliability characteristic.
Thermal step stress and isothermal aging studies can be used to estimate long term drifts of crystal parameter values in the operating system.

In a thermal step stress experiment changes in selected device parameters during a fixed interval time bake at increasing temperatures provide a signature for all thermally activated aging mechanisms of practical interest. Devices are cooled to room temperature for all measurements. Figure 3 shows a typical thermal step stress result for the resonance frequency of a thickness mode high quality quartz crystal device. For Figure 3 the fixed bake time interval is 16 hours (a convenient time interval) and the temperature step size is 20 degrees Centigrade. This thermal step stress result gives important information on crystal aging mechanisms on one device in about two weeks. All simple thermally activated effects are illuminated by the experiment. The shape of the curve in Figure 3 depends on the temperature step size, the step time interval selected, and on the distribution of aging mechanisms in the device being tested. Particular devices can be characterized quickly. The effects of device fabrication process changes and process accidents on device parameter aging can be determined quickly. This technique can be used to monitor the device fabrication process.

Figure 4 shows how a thermal step stress result can illustrate a processing problem with a given device. The peak at a temperature of 100 degrees Centigrade was caused by improper cleaning and drying during the fabrication process.

In isothermal aging studies sets of devices with assumed similar aging mechanisms (as suggested by thermal step stress results on samples from the set) are stored at various selected temperatures. At selected times the devices are cooled or warmed to room temperature and various device parameters are measured. Then each device is returned to its storage temperature. Electrical drive at frequencies near to or far from the resonance frequency can be applied during the storage. For each device parameter the shifts are fitted to the logarithm (or other related function) of the time at the storage temperature and extrapolated to the system end-of-life time. The logarithms of the end-of-life parameter values are fitted to the reciprocal of the absolute storage temperature (degrees Centigrade + 273.18). The slope of this fit is proportional to the activation energy associated with the dependence of aging rate on temperature. This activation energy may be different for different crystal parameters, i.e., resonance frequency or motional resistance. These results are used to estimate the changes in the distribution of crystal parameter values with time in the operating system. The distributions of extrapolated resonance frequency or crystal motional resistance are
sensitive functions of crystal device design, residual stress, and process cleanliness. These results can be used to calibrate the thermal step stress technique described above. In general the devices stored at lower temperatures (<80 degrees Centigrade) do not change much in short times (<6 months). The set of isothermal experiments therefore requires a large number of devices and a large number of measurements over a long period of time.

However, the isothermal aging results give the best estimate of the long term aging for any particular design of device and associated fabrication process. A typical isothermal aging plot for 80 degrees Centigrade is shown in Figure 5. A typical isothermal aging plot for 140 degrees Centigrade is shown in Figure 6. Typical results of extrapolated end-of-life resonance frequency are shown on an Arrhenius plot in Figure 7.

At selected times after package seal, the temperature coefficient of device parameters may give a useful measure of stress relaxation in the crystal device.

Failure modes on electrical, mechanical, and thermal overstress on sample devices give a strong indication of the consistency of the shipped product with the previously qualified product.

Residual gas analysis for sample packages selected at various points of the final testing process gives useful information on package seals and entire fabrication process cleanliness.

Process step yields and final electrical, mechanical, thermal, and temperature coefficient yields are all useful measures as to how closely the manufacturing process compares to the process used to fabricate the devices studied during the process qualification phase of the project.

During the entire qualification and manufacturing cycle, all device failures must be examined carefully to identify the causes of failure. There must be no unexplained failures in final qualification or in manufacture. This goal is very difficult to achieve.
CONCLUSION

In this paper some tools that can be used to plan for the manufacture of high reliability crystal devices have been discussed. In practice engineering judgements must determine whether the magnitude of a given observation generates a sufficient risk as to preclude the use of that device or batch of devices in the system. In this exercise, wishful thinking must give way to extremely objective thinking about the nature of the problem and the associated risk involved.

GENERAL REFERENCES


FIGURE 1
COST-RISK CURVE: BASIC

FIGURE 2
COST-RISK CURVES: TWO TECHNOLOGIES (A & B)
FIGURE 3
TYPICAL THERMAL STEP STRESS CURVE

Time Step = 16 hours

FIGURE 4
NON-TYPICAL THERMAL STEP STRESS CURVE

Time Step = 16 hours
FIGURE 5
ISOHERMAL AGING - 80 C.

\[ \frac{\Delta f}{f} \]

FIGURE 6
ISOHERMAL AGING - 140 C.

\[ \frac{\Delta f}{f} \]
FIGURE 7
ARRHENIUS AGING PLOT

slope proportional to activation energy

\[ \log \left( \frac{\Delta f}{f} \right) \]

\[ \frac{1}{(273.18 + \text{Temperature in degrees C.})} \]

Frequency changes must have same sign.

Frequency changes are extrapolated to a characteristic time such as system end-of-life.

Temperature is the aging temperature.